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Integration and High-Temperature Characterization of Ferroelectric Vanadium-Doped Bismuth Titanate Thin Films on Silicon Carbide

MATTIAS EKSTRÖM,[1,2] SERGIY KHARTSEV,[1] MIKAEL ÖSTLING,[1] and CARL-MIKAEL ZETTERLING[1]

1.—Department of Electronics, School of ICT, KTH Royal Institute of Technology, 164 40 Kista, Sweden. 2.—e-mail: mekstr@kth.se

4H-SiC electronics can operate at high temperature (HT), e.g., 300°C to 500°C, for extended times. Systems using sensors and amplifiers that operate at HT would benefit from microcontrollers which can also operate at HT. Microcontrollers require nonvolatile memory (NVM) for computer programs. In this work, we demonstrate the possibility of integrating ferroelectric vanadium-doped bismuth titanate (BiTV) thin films on 4H-SiC for HT memory applications, with BiTV ferroelectric capacitors providing memory functionality. Film deposition was achieved by laser ablation on Pt (111)/TiO_2/4H-SiC substrates, with magnetron-sputtered Pt used as bottom electrode and thermally evaporated Au as upper contacts. Film characterization by x-ray diffraction analysis revealed predominately (117) orientation. *P–E* hysteresis loops measured at room temperature showed maximum $2P_r$ of 48 $\mu C/cm^2$, large enough for wide read margins. *P–E* loops were measurable up to 450°C, with losses limiting measurements above 450°C. The phase-transition temperature was determined to be about 660°C from the discontinuity in dielectric permittivity, close to what is achieved for ceramics. These BiTV ferroelectric capacitors demonstrate potential for use in HT NVM applications for SiC digital electronics.

Key words: Ferroelectric, high temperature (HT), memory device, silicon carbide (4H-SiC), thin film, vanadium-doped bismuth titanate (BiTV)

INTRODUCTION

Ferroelectric $Bi_4Ti_3O_{12}$ (BiT) has several desirable properties for use in nonvolatile memory (NVM) applications compared with other well-studied ferroelectrics such as $Pb(Zr,Ti)O_3$ (PZT) and $SrBi_2Ta_2O_9$ (SBT). BiT is lead free, with higher remnant polarization (P_r) and lower processing temperature than SBT, and higher phase-transition temperature (T_c) than both materials (675°C for ceramics).[1] The properties of BiT can be further tuned by substitutional doping, at either A-site (Bi) with lanthanides or B-site (Ti) with transition metals, or both.

B-site substitution can effectively reduce leakage current and improve ferroelectric properties, and experimental work has been done on Nb,[2,3] V,[2–7] W,[2] and Mo.[8] In a comparison between different B-site dopants, V-doped BiT (BiTV) was shown to have lower leakage currents than BiT doped with W or Nb.[2] Dopants with higher valency than Ti (such as V^{5+}) neutralize oxygen vacancies by donating electrons, which results in reduced conductivity and domain pinning.[5] Doping can enhance polarization by decreasing the amount of crystal *c*-axis orientation of deposited films.[2] High polarization requires non-*c*-axis orientation, as the major polarization component is along *a*-axis, with saturation P_s of 50 $\mu C/cm^2$.[1] Small amounts of V doping ($x \sim 0.01$ in $Bi_{4-x/3}Ti_{3-x}V_xO_{12}$) slightly reduce T_c by several

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kelvin.[4,5] This small reduction is in contrast to A-site doping, which can reduce T_c by several hundred kelvin.[9] BiT films doped at A-site with elements such as La[10] or Nd[11,12] exhibit good polarization and fatigue properties.

The high T_c of B-site-doped BiT enables NVM applications at high temperature (HT). Although A-site-doped BiT films show good performance, their T_c is too low for HT applications. Its high remnant polarization (>10 $\mu C/cm^2$) makes BiT more suitable for one transistor (1T)–one capacitor (1C) or 2T–2C operation than for 1T operation.[13] Although it is possible to investigate the HT ferroelectric properties of ceramics and thin films on glass substrates, for device applications, it is desirable to demonstrate the properties of thin-film capacitors on semiconductor wafers. The semiconductor wafer influences the growth of ferroelectric films as well as their properties, such as thermal conductivity and expansion. The wafer provides a mechanical boundary condition that induces stresses in the film. Stresses can clamp the film or induce strain that modifies the ferroelectric properties, in accordance with Ginzburg–Landau theory.[14] The semiconductor material should at the same time enable use of HT electronics.

4H-SiC enables HT electronics through its wide bandgap (E_g) of 3.2 eV. Digital electronics have been demonstrated to operate up to at least 400°C for complementary metal–oxide–semiconductor (CMOS) field-effect transistors,[15] 500°C for junction field-effect transistors (JFETs)[16] and 600°C for emitter coupled logic (ECL, a logic family that uses bipolar junction transistors).[17] Previous efforts to integrate ferroelectrics on SiC include PZT[18,19] and $BaSrTiO_3$,[20] with PZT evaluated for HT NVM applications with memory functionality up to 200°C. Combining SiC digital electronics with high-T_c ferroelectrics is a possible approach to construct microcontrollers which can operate at HT, where the NVM stores programs. Such microcontrollers could be used to control other HT electronics, such as various sensors and amplifiers. HT electronics are beneficial for a large variety of applications, such as automotive, aerospace, gas sensing, deep-well drilling, power electronics, and space exploration.[21]

Ferroelectric processing takes place after the HT front-end-of-line (FEOL) but before the low-temperature back-end-of-line (BEOL). A commonly cited[3,7,10] advantage of BiT compared with SBT is the low processing temperature, which is in the range from 650°C to 750°C.[2,3,7,10,11] However, this processing temperature could still be too high for modern silicon very-large scale integration (VLSI, more than 10^9 transistors on a chip), for which the thermal budget may be lower than 600°C after nickel salicidation. Integration of BiT for NVM applications requires process compatibility with the transistor technology. Current SiC electronics, especially for HT applications, can have a thermal budget of 800°C or higher after contact alloying. As such, the typical BiT process temperature range is not expected to adversely affect SiC transistors.

We demonstrate herein the possibility of integrating thin-film ferroelectric BiTV by pulsed laser deposition (PLD) on SiC substrates, exhibiting hysteresis up to at least 450°C. PLD is an excellent deposition method for growth of high-quality crystalline oxides. Li et al.[22] recently showed that Nd-doped BiT can be uniformly deposited on 125-mm silicon wafers by PLD, making this method interesting for production on standard 100-mm SiC wafers. Other scalable production methods include chemical solution deposition (CSD) methods, such as sol–gel.[2,3] The experimental results are primarily compared with the results of Choi et al.,[2] who used the same metal–ferroelectric–metal (MFM) device structure on silicon, with the difference of using CSD. MFM capacitors are expected to show better stability over a wide range of temperature as compared with metal–ferroelectric–semiconductor (MFS) capacitors. Use of MFS capacitors for 1T–1C operation requires as high doping as possible to minimize depletion and resistivity. Even if typical high device doping (10^{19} cm^{-3} to 10^{20} cm^{-3}) were to be used, the high polarization of BiT (>10 $\mu C/cm^2$) would give rise to a depletion region of the order of $\sim$10 nm (for metals, the corresponding length is the Thomas–Fermi screening length,[14] which is 0.01 nm to 0.1 nm). The depletion region acts as a small dielectric capacitor in series with the large ferroelectric capacitor. The depletion capacitance leads to voltage drops and a depolarization field. SiC–dielectric interfaces are notoriously defect dense, and it is likely that the SiC/BiTV interface is poor with numerous interface and/or near-interface traps. Addition of insulating or buffer layers between SiC and BiTV would contribute to the depolarizing field and voltage drops. It might be assumed that the performance of MFMs on silicon is comparable to that of MFMs on SiC, despite the mechanical and thermal differences between silicon and SiC. The benefit of using SiC substrates in this study is that there is no need to assume equal performance, because the performance of MFMs on SiC is evaluated directly.

The next section presents the details of the experiment. The results are divided into two parts. The first part presents structural analysis. The second part reports electrical characterization, split into a room-temperature (RT) and a HT section. Finally, we present the conclusions of our study.

EXPERIMENTAL PROCEDURES

The PLD target was prepared by standard solid-state reaction using 99.99% pure Bi_2O_3, TiO_2, and V_2O_5 as starting materials. Powders were mixed in stoichiometric ratio in ethanol for 2 h. Bismuth can be lost during HT processing due to its volatile nature. To compensate for losses, 5% extra Bi_2O_3

was added. The mixture was calcined at 780°C in air for 5 h, reground, and uniaxially pressed into a pellet. The pellet was sintered in air at 920°C for 2.5 h, which resulted in a density equal to 94% of its theoretical value. The nominal stoichiometry of the BiTV target was $Bi_{3.98}Ti_{2.94}V_{0.06}O_{12}$.

Substrates were prepared by dicing 4H-SiC wafers (100 mm, *n*-type doped, Si-face standard polish epiready, 4° off-axis) into 10 mm × 10 mm pieces. After dicing, the substrates were cleaned in Piranha (3:1 H_2SO_4:H_2O_2 volume ratio) for 5 min, rinsed with deionized water, 2 min IMEC [100:1:1 H_2O:HF (50%):$CH(CH_3)_2OH$], rinsed, and blown dry with N_2 gas. All further processing was done on the Si-face.

The bottom Pt electrode was deposited using radiofrequency (RF) magnetron sputtering. To promote adhesion to the substrate, a 20-nm layer of TiO_2 was deposited using reactive sputtering with Ti and Ar/O_2 gas mixture (4:1 flow ratio) at 550°C, 670 mPa, and 60 W of RF power. Pt (200 nm) was deposited, without breaking vacuum, in pure Ar at 400 mPa and 40 W. The distance from both magnetrons to substrate was kept at 30 mm. The Pt films were annealed *in situ* at 550°C for 5 min in argon flow.

A COMPex 110 KrF (248 nm) excimer laser was used to ablate the BiTV target. The target was rotated and rastered during the ablation process to avoid wearing, pitting, and change in plume direction. The deposition rate was 0.1 nm/shot for laser energy density of ~3 J/cm^2, substrate to target distance of 5 cm, oxygen pressure of 9.3 Pa, substrate temperature of 470°C, and repetition rate of 20 Hz. Postdeposition annealing was carried out *in situ* at 650°C, being the highest temperature used in this process, for 5 min in oxygen atmosphere at 80 kPa. The film thickness was 185 nm with root-mean-square (RMS) surface roughness less than 2 nm.

The upper electrodes were 200-nm-thick gold films thermally evaporated through a shadow mask. The openings were circular with diameter of 250 μm (area about 4.9×10^{-4} cm^2). The electrodes were annealed in air at 450°C to reduce leakage current.

A schematic of the MFM capacitor is shown in Fig. 1. The capacitors have individual top contacts and share one common bottom electrode. The TiO_2 film electrically decouples the capacitors from the substrate.

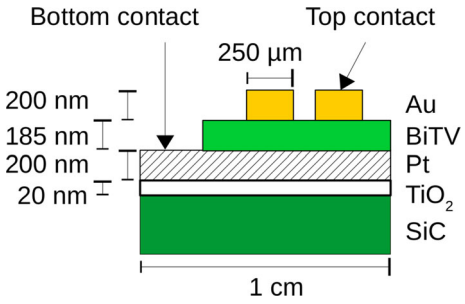

Fig. 1. Schematic of ferroelectric capacitors on SiC (not to scale).

The films were characterized by θ–2θ scan x-ray diffraction (XRD) using an Empyrean x-ray diffraction system (PANalytical) with Cu K_α radiation. A Tencor P-15 was used to determine film thickness and surface roughness. The temperature and frequency dependences of dielectric properties as well as capacitance–voltage (*C*–*V*) traces were recorded using a Philips PM6304, a Keithley 2002 multimeter, and a Keithley 2200 source meter. *P*–*E* hysteresis loops were recorded with a 1-pC-resolution electrometer while sweeping the applied voltage in a continuous triangular waveform at frequencies from 20 Hz to 80 kHz. A programmable Keithley 6517A electrometer was used to measure current–voltage (*I*–*V*) characteristics.

RESULTS AND DISCUSSION

Structural Characterization

Figure 2 shows the results of θ–2θ XRD measurements. In spite of Bi volatility, no foreign phases, such as pyrochlore $Bi_2Ti_2O_7$, were detected. The strongest BiTV peak was (117), being stronger than the (00*l*) peaks by two orders of magnitude. The degree of *c*-axis orientation is typically estimated as $I(006)/[I(006) + I(117)]$, where $I(006)$ and $I(117)$ are the intensities corresponding to (006) and (117) peak, respectively.[2] The (006) signal was either absent or lower than the noise floor, indicating a degree of *c*-axis orientation below 1%. There are other weak peaks corresponding to non-*c*-axis planes, such as (111), (200), and (228). The mix of peaks indicates that the films were polycrystalline, and either randomly oriented or predominately (117) oriented. Compared with Choi et al.,[2] the amount of *c*-axis orientation is much smaller (cf. 83.6%). This difference in preferred orientation could be due to the different deposition method used. The films were also annealed at higher temperature (cf. 700°C) for longer time (cf. 30 min), which could contribute to the difference in crystallization.[7]

The properties of the adhesion layer affect both the Pt layer and the ferroelectric layer.[23,24] The TiO_2 adhesion layer used in this study was investigated by depositing a 120-nm-thick TiO_2 film on SiC, as described in the previous section, followed by XRD measurements. The XRD results (not shown) did not reveal any crystallinity of the deposited film. The possibility of the film being amorphous cannot be excluded. The Pt films on the regular adhesion layers showed only (111) peak with full-width at half-maximum less than 0.1°.

Electrical Measurements

Room Temperature

Figure 3 shows the dielectric permittivity and loss tangent spectra of the BiTV film. The

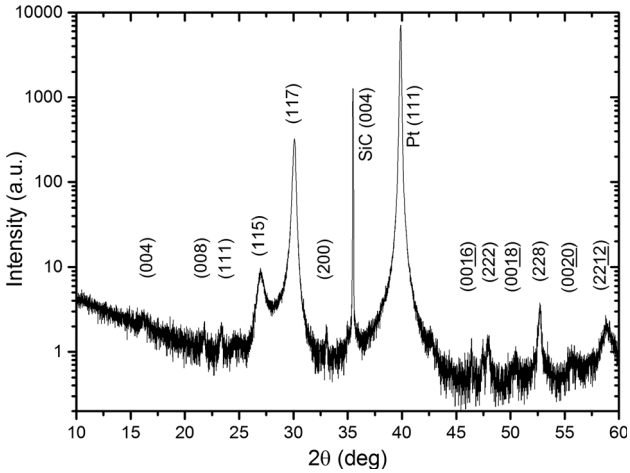

Fig. 2. θ–2θ XRD results. The strongest BiTV peak corresponds to (117). There are several weak (00*l*) peaks together with non-*c* axis peaks. No foreign phases are present.

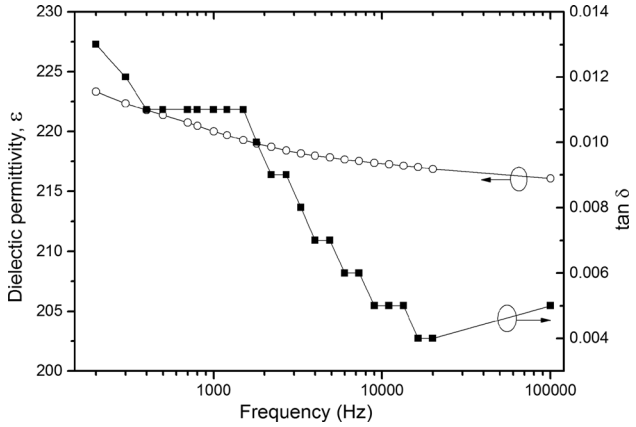

Fig. 3. Dielectric permittivity and loss tangent for BiTV. The capacitor shows weak frequency dependence. The loss tangent is low for all frequencies, indicating a high-quality reactive component.

permittivity decreased continuously from 100 Hz to 100 kHz, with dielectric permittivity of 223 at 100 Hz. The loss tangent was in the range of 0.013 for low frequencies and 0.004 for high frequencies. The weak frequency dependence and low loss indicate that the measured impedance is dominated by the capacitive reactance for these frequencies.

To investigate steady-state leakage, the current was sampled 3 s after the voltage application. The upper subplot in Fig. 4 shows the leakage current as a function of applied electric field. The leakage is quite asymmetric, which can be attributed to the use of different metal electrodes. The leakage at $\pm$100 kV/cm is of the order of 10^{-8} A/cm^2, comparable to or better than some previous results for BiTV.[2,5–8] Compared with Choi et al.,[2] the leakage is lower (cf. 7×10^{-6} A/cm^2). The lower subplot in Fig. 4 shows the dielectric permittivity butterfly curve. It is fully opened for peak electric fields larger than 600 kV/cm. The full opening corresponds to saturated *P*–*E* hysteresis loop (Fig. 5). The leakage increases by several orders of magnitude above 300 kV/cm. The applied electrical field should not be much larger than said field for reliable operation. The need for large fields (>600 kV/cm) to saturate the *P*–*E* loop is in conflict with reliable operation. As such, actual operation should be limited to minor loops.

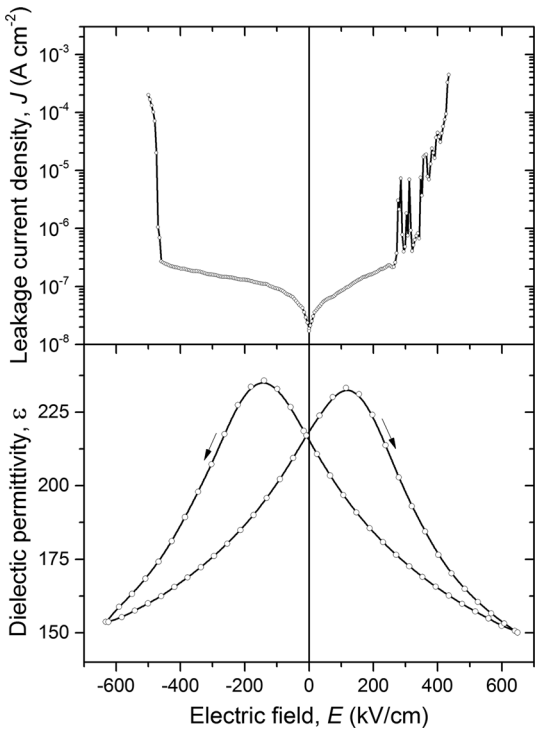

Fig. 4. Upper subplot: leakage current versus applied electric field; lower subplot: dielectric permittivity. The leakage increases significantly above 300 kV/cm. The permittivity shows the ferroelectric butterfly curve.

Figure 5 shows a family of *P*–*E* loops. The applied voltage was continuous bipolar triangular pulses at frequency of 2 kHz. The coercive field (E_c = 209 kV/cm) is much higher than that in single crystal (~50 kV/cm). One explanation could be thin-film effects, such as surface domain wall pinning or metal/ferroelectric depletion region(s).[25] Another explanation could be that the electric field component along the *a*-axis is small due to the predominant (117) orientation. The coercive field shows asymmetry, which again is attributed to the use of different metals as electrodes. Compared with Choi et al.,[2] the coercive field is significantly larger (cf. 65 kV/cm).

The *P*–*E* loop shows saturation at peak electric fields larger than 600 kV/cm. The highest remnant polarization ($2P_r$) of the hysteresis loop is about 48 μC/cm^2. This is much larger than that obtained by Choi et al.[2] (cf. 29 μC/cm^2), which could be explained by the high *c*-axis orientation in their film. The result is comparable to Chaudhuri et al.[7] (cf. 42 μC/cm^2).

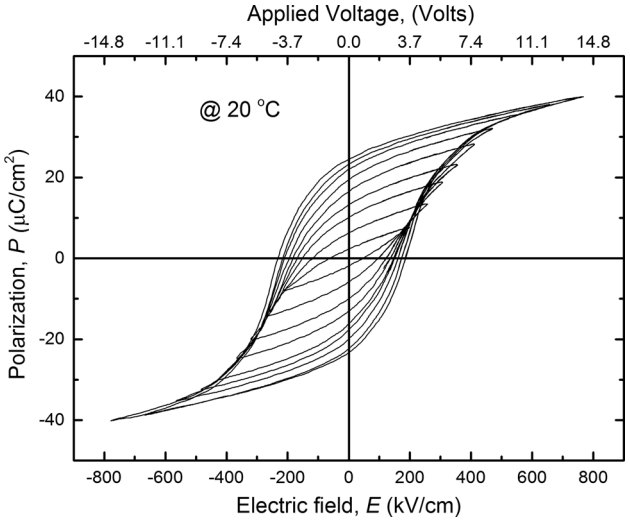

Fig. 5. Family of *P*–*E* loops at 20°C. Minor loops are present for 200 kV/cm. The major loop appears for fields larger than 600 kV/cm. The polarization saturates at 40 μC/cm^2. The coercive field and remnant polarization for the major loop are 209 kV/cm and 24 μC/cm^2, respectively.

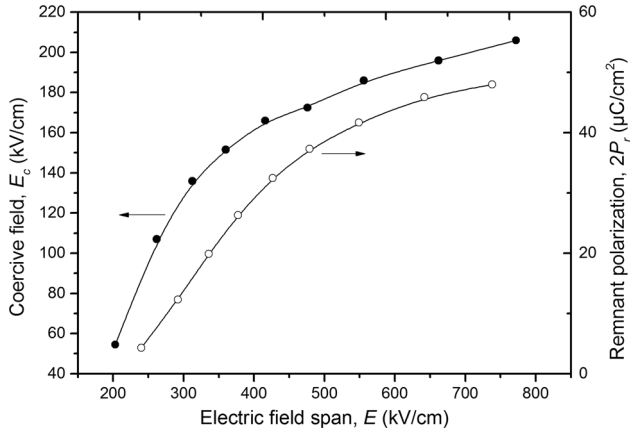

Fig. 6. Coercive field and remnant polarization of minor hysteresis loops. Both parameters increase with peak field and saturate above 600 kV/cm.

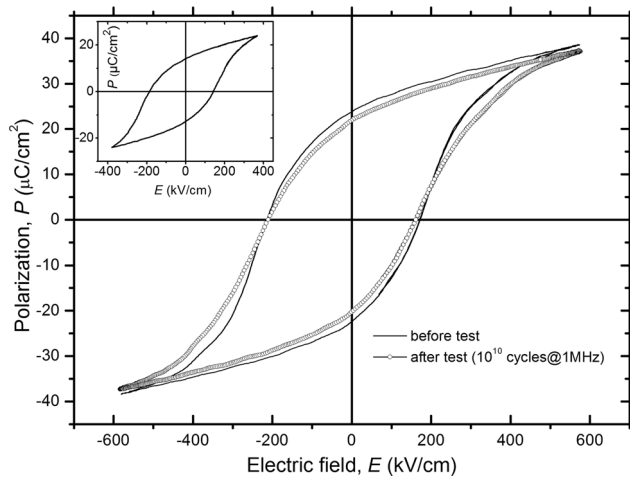

Fig. 7. Endurance test. The inset shows the fatigue cycle. The solid curve shows the fresh hysteresis loop, while the curve marked with circles shows the postfatigue curve after 10^{10} cycles. The remnant and saturation polarization decreased due to fatigue.

In Fig. 6, the coercive field and remnant polarization are plotted for the minor loops in Fig. 5. For 1T–1C operation at the 0.5-μm technology node, the capacitor area and the switched polarization (corresponding approximately to $2P_r$) are 3 μm^2 and 30 μC/cm^2, respectively.[13] From Fig. 6, the capacitor reaches 30 μC/cm^2 above 400 kV/cm, corresponding to read/write voltage of 7.4 V. Such a read/write voltage would be small for the SiC power supply, which is in the range of 10 V to 15 V.[15–17] SiC technology at 1 μm could have capacitors with minimum size of 12 μm^2. Assuming a capacitor over field oxide (COFO) design and relaxed transistor design rules, the minimum amount of memory for a standalone chip (7 mm × 7 mm) is of the order of 1 Kib to 8 Kib (average areal density 20 b/mm^2 to 160 b/mm^2). This density is limited by current transistor technology rather than the ferroelectric capacitor. To put this density in perspective, the first ferroelectric NVM integrated with silicon CMOS had 256 b for chip size of 4.0 mm × 3.2 mm (average areal density 20 b/mm^2).[26]

To investigate the endurance of the capacitors, a capacitor was switched repeatedly with bipolar triangular pulses of 375 kV/cm at 1 MHz. The *P*–*E* loop was measured at 2 kHz before and after switching 10^{10} times. Figure 7 shows the loops, and the inset illustrates the switching fatigue. A clear degradation is observable in the remnant polarization, with a $2P_r$ decrease of 9.3% (from 46.5 μC/cm^2 to 42.2 μC/cm^2). Degradation was also reported by Choi et al.[2] after 10^{10} cycles, with degradation of about 20% based on their pulse measurement of the switched polarization. The difference in the amount of degradation is most likely due to differences in the fatigue cycles. The overall loop shape is the same before and after fatigue cycling.

High Temperature

The leakage current can cause current-induced degradation. This is detrimental to device reliability and must be minimized. Figure 8 clearly shows that the steady-state leakage current increased with temperature. Different maximum electrical field strengths must be used at different temperatures if the target application requires a maximum leakage current rating.

No single thermally activated conduction model, such as Schottky or Poole–Frenkel emission, can be fit for the entire measured temperature range. Different mechanisms may dominate for different temperature ranges.

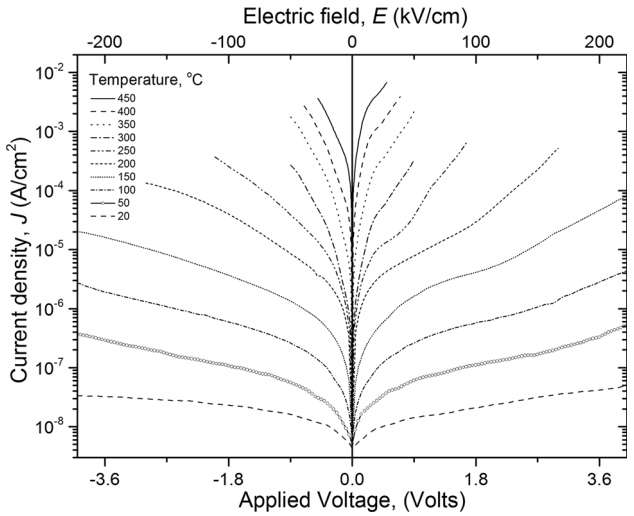

Fig. 8. Leakage current density at different temperatures, as a function of applied voltage/electric field. The leakage increases with increasing temperature. The upper voltage bound is reduced at each temperature to prevent dielectric breakdown during measurement. The capacitors are operational at fields larger than shown here.

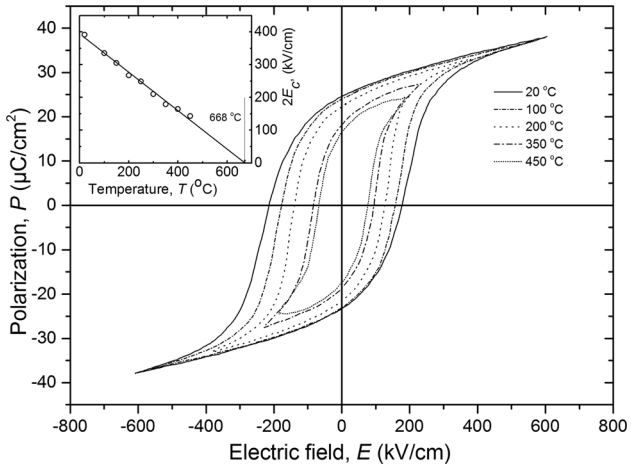

Fig. 9. Hysteresis loop at several different temperatures. Both the coercive field and polarization decrease with increasing temperature. The inset shows the coercive field versus temperature.

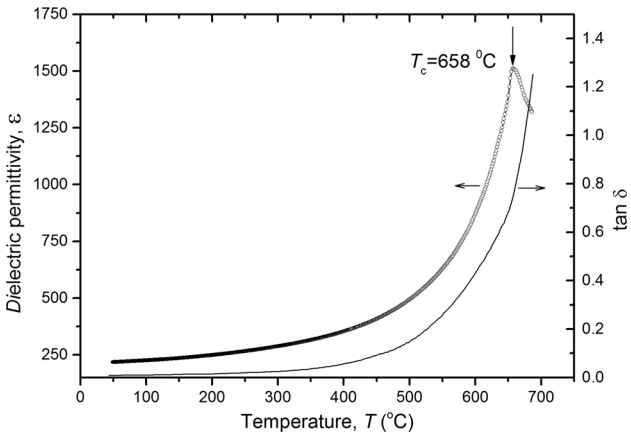

Fig. 10. Dielectric permittivity ε_r and tan δ versus T measured at 100 kHz. The permittivity increases and becomes discontinuous at T_c. The discontinuity marks the ferroelectric to paraelectric phase transition.

The P–E hysteresis loop was measured at 10 kHz at nine different temperatures ranging from 20°C to 450°C. The loops are plotted for five temperature points in Fig. 9. The remnant polarization decreased with temperature, but the read margins were still adequate at HT. The coercive field decreased with temperature, enabling lower read/write voltages at higher temperatures.

The coercive field vanishes at the paraelectric phase transition. The inset in Fig. 9 shows that simple linear extrapolation gives a transition temperature of 668°C, close to the expected value. The transition temperature for BiT ceramics is 675°C, and previous studies[4,5] reported a phase-transition temperature for BiTV ceramics of 672°C.

For memory applications, it is possible to design the circuit to use a single read/write voltage for a specific temperature or a very narrow temperature window. However, this will be challenging for a very wide temperature window, e.g., RT to ~400°C. Given that the leakage increases and the coercive field decreases with increasing temperature, one strategy is to use a voltage reference-like circuit with appropriate complementary to absolute temperature (CTAT) properties to set the read/write voltage to decrease with temperature.

The capacitance and loss tangent were recorded with an alternating-current (AC) small signal (100 kHz) during a temperature ramp to find the transition temperature. Figure 10 shows the results. The dielectric permittivity increased with temperature and changed discontinuously at 658°C, indicating a phase transition. No attempt was made to investigate whether this transition was first order or continuous.

The dissipation increased rapidly with increasing temperature. The P–E loop could not be measured above 450°C ($0.78 \times T_c$) due to the losses (loss tangent > 0.1).

CONCLUSIONS

We have demonstrated BiTV MFM capacitors integrated on SiC. The performance of the capacitors is comparable to what has already been demonstrated on silicon substrates. The remnant polarization, determined from P–E loops, gives wide read margins for 1T–1C or 2T–2C operation. The capacitors show fatigue after 10^{10} cycles, with 9.3% degradation in $2P_r$. P–E loops are measurable up to 450°C, while measurements above this temperature are limited by losses. The leakage current increased with temperature and could cause reliability issues unless minimized. A single read/write voltage can be used for a targeted temperature or narrow temperature window, whereas wide temperature

(RT to ~400°C) operation will require circuits with CTAT output to adjust the voltage. The fundamental temperature limit is around 660°C, where the ferroelectric transitions to paraelectric state. These BiTV MFM capacitors show properties which indicate that they could possibly function as NVM devices for HT applications.

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